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REALIZATION OF DIRECT DIGITAL SYNTHESIS IN CORDIC ALGORITHM

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ABSTRACT

Nowadays the modern communication system and software defined radio-based applications needs Trans receiver consisting of fully programmable circuit which performs modulation and demodulation process. The method which does not need memory for realizing modulators and demodulators is CORDIC algorithm. The CORDIC algorithm is a versatile algorithm which calculates only adder and shifter operations instead of using multiplier. So, this algorithm is mostly used for VLSI and digital signal processing. The main concept used in this project is Direct Digital Synthesis (DDS) which generates the analog waveform in digital format based on CORDIC algorithm approach .This paper focuses on analysis and simulation of Binary phase shift keying (BPSK), Binary amplitude shift keying (BASK), Binary frequency shift keying (BFSK), Quadrature phase shift keying (QPSK) modulation scheme using DDS based on CORDIC algorithm instead of ROM look up table which greatly reduce the number of slices and no of look up tables. The whole simulation is done on Modelsim and Xilinx-ISE using Verilog descriptive language and these modulation schemes are implemented on Spartan-3 FPGA kit.

INTRODUCTION

Software Defined Radio (SDR) is an important method where components are implemented in hardware instead of implemented in terms of software. SDR is a trans

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receiver system in which DDS based CORDIC is an important block which generates the cosine and sine waveforms. To improve the SDR in terms of area and time, many techniques are used. One of the techniques to design DDS is Co-ordinate Rotation Digital Computer (CORDIC) method is used for the creation of cosine and sine waveforms.

DDS is an important method which generates waveforms in digital form. Direct digital synthesis is a method under the classification of frequency synthesizer used for producing waveforms from single, fixed reference clock. DDS has been considered as a superior technique for generating accurate, frequency agile and low distortion waveform. DDS is implemented by using algorithm called CORDIC. This algorithm calculates the pseudo rotation of two-dimensional vector by using adder and shifter operations. In this paper, CORDIC based DDS is proposed. This paper presents how to use CORDIC algorithm in the implementation of DDS. The simulation of various modulation schemes such as BASK, BFSK, BPSK, QPSK using CORDIC based DDS is done and implemented in SPARTAN- 3 FPGA kit.

DIRECT DIGITAL SYNTHESIS

DDS is an important method which produces arbitrary waveforms. Compared with the other frequency synthesizer, it has many advantages including high resolution, high frequency conversion speed, phase continuous and low phase noise. These advantages make the DDS is widely used in digital signal as the signal generator source. An implementation process of novel type DDS based on CORDIC algorithms is proposed. So, the circuit is simple and easy to realization. The novel method can accurately produce the cosine and sine output waves and can satisfy the requirements of high speed, accuracy, high resolution, and real-time computing. Compared to the traditional DDS, the novel type DDS based on CORDIC algorithm has lower resource consumption and greatly improved performance and speed.

CONCEPT OF CORDIC

Co-ordinate Rotation Digital Computer (CORDIC) is an iterative and versatile algorithm which uses pseudo rotations to calculate elementary functions. CORDIC uses adder and shifter operations instead of using multiplier which greatly reduces the complexity. CORDIC performs several functions such as the calculation of trigonometric, logarithmic, exponential functions etc. CORDIC works on two modes such as vectoring mode and rotation mode.

Vectoring mode: In this type of mode the y-axis of the input vector is required to be zero. So, this mode calculates the phase and magnitude of the input vector.

Rotation mode: In this type of mode, the θ component is required to be zero and this mode calculates the plane rotation of the input vector.

MATHEMATICAL MODEL OF CORDIC

Consider a input vector Ei(Xi,Yi) which is rotated by an angle αi then the new vector becomes Ei+1(Xi+1 ,Yi+1).

The following iteration equations are

xi+1 = xi cos αi – yi sin αi;

yi+1 = xi sin αi + yi cosαi;

θi+1 = θi+ αi;

Then the above equation becomes

xi+1 = cos αi (xi– yi tan αi);

yi+1 = cos αi (xi tan αi + yi);

Replace tan αi = di 2^-i

where di = {-1,1} => {di = +1, clockwise direction

di = -1, anticlockwise direction}

Then the above equation becomes

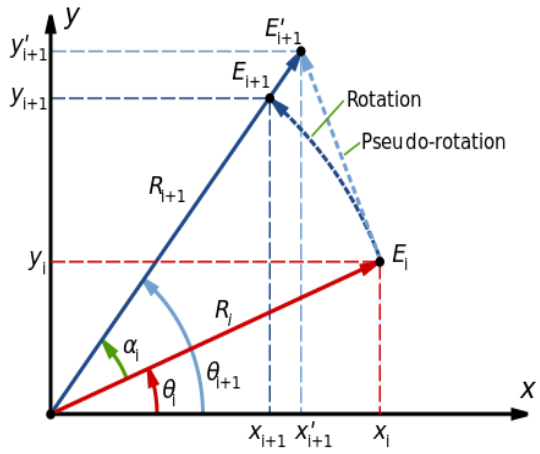
xi+1 = K (xi - di2^-i yi);

yi+1 = K (yi + di2^-i xi);

θi+1 = θi- diαi;

Here K is the scale factor to simplify the algorithm which allows pseudo rotations then the cos α is term was omitted.

Figure – 1: *Mathematical Model of CORDIC*



Using CORDIC in rotation mode

xi+1 = cosαi (xi - 2^-i yi)

yi+1 = cos αi (yi + 2^-i xi)

zi+1= zi- di αi;

CORDIC performs several micro rotations by the angles

αi = tan-1(2^-i) where αi is the fixed elementary angles.

After n iterations when Zn is sufficiently close to 0, then we have Z = $\sum\alpha_i$ and

Xn = K (X cos Z – Y sin Z) where K = 1.646 760258……..

Yn = K (Y cos Z + X sin Z)

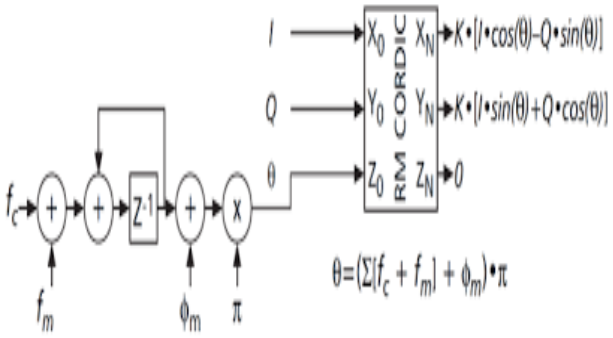
Zn = 0

The range of convergence is 0° ≤ Z ≤ 99.7°. Outside this range, we can use trig identities to convert to the range

cos (Z- π) = -cos Z;

sin (Z- π) = sin Z;

Figure – 2: *CORDIC in Rotation Mode*

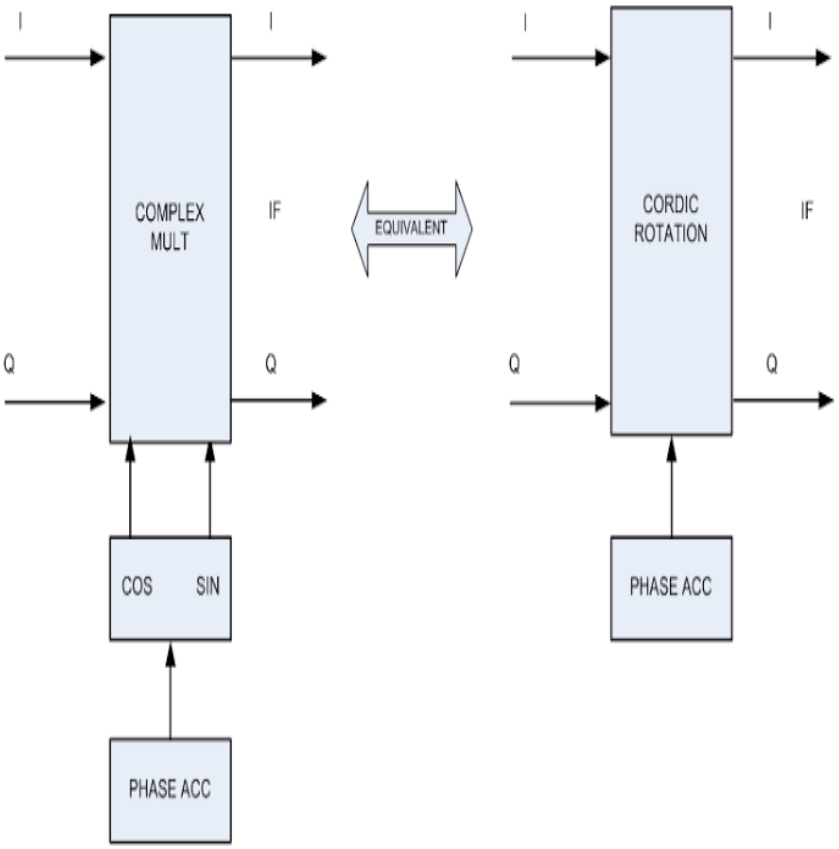


Here CORDIC works on rotation mode. CORDIC consists of three inputs X0, Y0 and Z0. It also having three outputs Xn, Yn and Zn. Here CORDIC acts as a oscillator to produce a sine and cosine signal.

SCOPE OF WORK

In existing system, the DDS is implemented in multiplier circuit. Here Complexity is high. It takes more area and having less efficiency. To solve the above-mentioned difficulties, the proposed architecture of DDS using CORDIC is simulated by means of Verilog HDL and implemented in terms of FPGA with less area requirement and to increases the speed. The major advantage of using CORDIC in DDS is to reduce the ROM size.

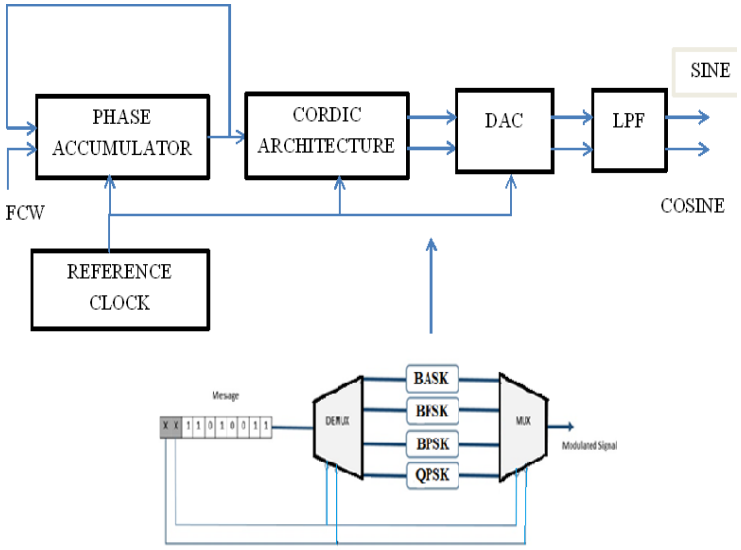
Figure – 3: *Equivalent Circuit of CORDIC*



PROPOSED SYSTEM

6.1 Block Diagram of DDS

Figure – 4: *Block Diagram of DDS*



An implementation processes of novel type DDS based on CORDIC algorithms is proposed. Therefore the circuit is simple and easy to realization. Here one 4:1 multiplexer and one 1:4 demultiplexer is used. Here there are four modulation schemes such as BASK, BFSK, QPSK and BPSK. There are 10 bits of message signal where first two bits consists of selection line and remaining 8 bits are treated as a message signal. It having four combinations are 00, 01, 10, 11. The above mentioned 2 bits are entered into the demultiplexer. 00, 01, 10, 11 combinations are entered serially in the demultiplexer. Now the modulation schemes are selected as per selection lines combination are entered into demultiplexer through message bits. Now modulation schemes are choosed from the above such as either BASK, BFSK, QPSK or BPSK with their modulated output combination are entered into multiplexer. Here by means of multiplexer, any one of modulated scheme is selected. The final output is a modulated sinusoidal waveform according to the selection lines combination of modulation technique.

Table – 1: *Selection of Modulation Scheme*

Selection Lines	Modulation Schemes
00	BPSK
01	BASK
10	BFSK
11	QPSK

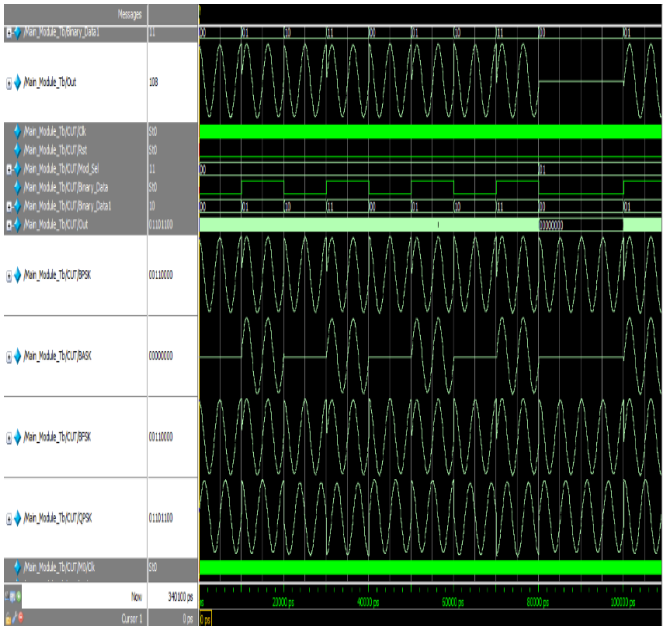
RESULTS AND ANALYSIS

7.1 Binary Phase Shift Keying

Here the phase of the carrier is varied in accordance to binary data. 0° for binary 1 and 180° for binary 0. Here the pair of signals is given that differ only in phase of 180° are known as antipodal signals.

7.1.1 Simulation Output of BPSK

Figure – 5: *Simulation of BPSK*

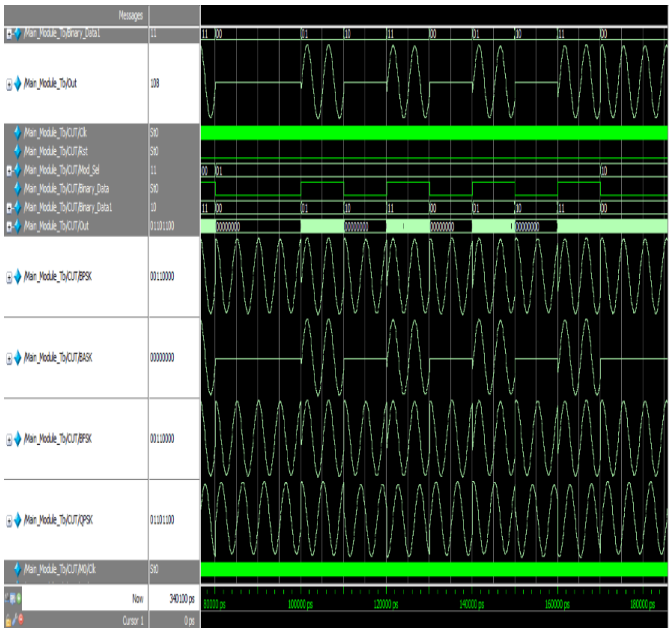


7.2 Binary Amplitude Shift Keying

In BASK, the amplitude of the sinusoidal carrier signal is changed according to the message level ("0" or "1"), while keeping the phase and frequency constant.

7.2.1 Simulation Output of BASK

Figure – 6: *Simulation of BASK*

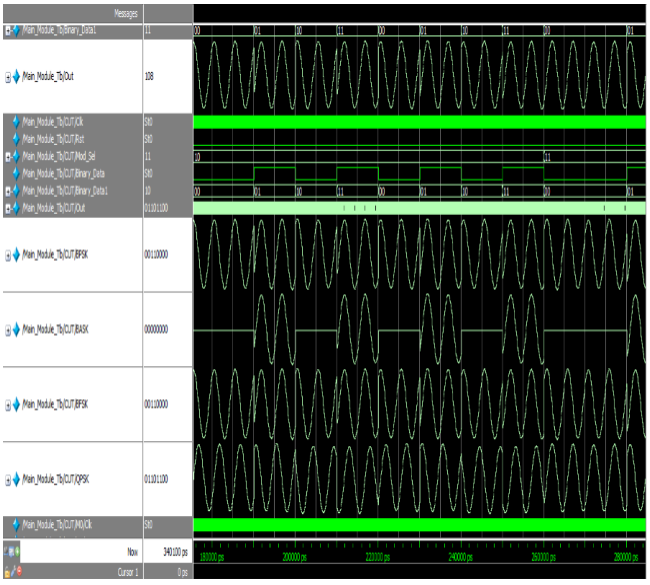


7.3 Binary Frequency Shift Keying

In BFSK, the frequency of the carrier is varied accordance to the binary data where amplitude and phase remains constant. In BFSK, symbols 1 and 0 are distinguished from each other by transmitting one of the two sinusoidal waves that differ in frequency amount.

7.3.1 Simulation Output of BFSK

Figure – 7: *Simulation of BFSK*



7.4 Quadrature Phase Shift Keying

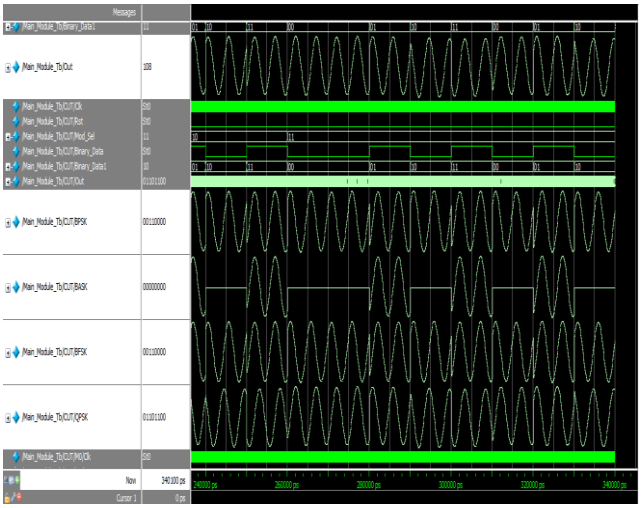
Here the phase of the carrier taken one of four equally phases value as π/4, 3π/4, 5π/4, 7π/4 which produces modulated wave

Table – 2: *Phase Shift of QPSK*

No. of Bit Combination	Phase Shift
00	0°
01	180°
10	90°
11	270°

7.4.1 Simulation Output of QPSK

Figure – 8: *Simulation of QPSK*



7.5 Comparison Table between Existing and Proposed System

Table – 3: *Comparison Table between Existing and Proposed System*

Method Name		Area in Number of Lut		Delay		
Spartan 3 XC 3S200TQ144	**Gates**	**Flip Flops**	**Input/Output Blocks (IOBs)**	**Delay**	**Gate or Logic Delay**	**Path or Route Delay**
LUT Based DDS	1,98,81,3	90	77	10.298ns	6.896ns	3.402ns
CORDIC Based DDS	2159	64	15	10.250ns	6.565ns	3.105ns

7.6 Device Utilisation Summary

Table – 4: *Summary of Device Utilisation*

System Analysis	No. of LUTs	No. of Slices	Total Gate Count for Design
Existing System	161	81	1,98,813
Proposed System	154	77	2159

CONCLUSION

This paper gives the usage of CORDIC algorithm in direct digital synthesis. This paper emphasizes the Direct Digital Synthesizer using CORDIC which having less area to implement in FPGA which increases the speed and reduces the delay. This paper reveals that the CORDIC algorithm is used by means of DDS to implement different communications systems such as BPSK, BASK, BFSK, QPSK in Verilog HDL. This paper also describes CORDIC based DDS which reduces the number of LUT and number of slices which requires lower resource consumption and greatly improved performance and speed.

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